REMARKS

This communication is responsive to the Final Office Action of April 21, 2005in which the following objections were raised: [2-3] Claim 1-6 were rejected under 35 U.S.C. 102(e) as being anticipated by Castellano (US Patent 6,674,750).

Applicant has Amended Claim 1-6.

2-3. **CLAIM 1 REJECTED UNDER 35 U.S.C. 102(e):**

Claims 1-6 were rejected under 35 U.S.C. 102(e) as being anticipated by Castellano. (US Patent 6,674,750).

In the Final Office Action of 4/21/2005 the Examiner stated that "...Castellano discloses a system and a method for provisioning packet based communication channels and time-division multiplexed (TDM) communications channels on a subscriber line." (Final Office Action at page 2). The Applicant respectfully rejects that characterization as it applies to a subscriber line.

The Castellano reference discloses a method for arbitration of data on a TDM backplane bus of a Network Attached Switch coupled to a plurality of synchronous and packet based interface modules. "...[T]he present invention is ...directed to a method and apparatus for communicating both packet data and time division multiplexed (TDM) transmissions over a shared TDM bus" (Castellano at col 6, lines 21-24). Castellano's bus includes discrete signal lines for data and for packet inhibits 1-2. (See FIG. 7 and col. 16 lines 37 to Col 17 line 55). It would also appear that the Castellano bus as with all busses includes a common clock identified for example in FIG. 4A reference 455 as a '*TDM frame pulse*'. In the Castellano disclosure synchronization of TDM frame boundaries between sending and receiving devices is not an issue because the bus includes a common clock referred to as the TDM frame pulse accessible to all devices coupled to the bus. "*The time slot control function*

is synchronized with the system TDM frame pulse 455, and is used to determine which location in the time slot map 454 should be accessed."(Castellano at col. 9, line 65 to col 10 line 1).

The synchronization issues which Castellano does address are related to enhancing the ability of the packet interface units to utilize the bus without the requirement of propagating a time slot map to each. This is accomplished by yet another dedicated bus line, identified as the buffer enable signal. "*This buffer enable signal ...is also driven on the backplane bus indicating that TDM data is currently being transmitted for this time slot. This signal is wired-ANDed across all modules....This signal is the Packet Inhibit #1 signal ...defined in this invention, which is used to suspend transmission of packet data between Packet Interface Modules....*"(Castellano at col. 10 lines 14-25).

In the Applicant's claimed invention by contrast a communication medium modulated with an X-DSL communication protocol forms the data transport medium. There is no bus coupling the modems. The clock and recovered clock that the modems share is **not** synchronous with the TDM frames that are carried with the X-DSL communication channel. The reason for this is that X-DSL data rates vary depending on the available symbol rate and the number of bits per symbol, parameters which will vary depending on the length of line, line quality etc. (Applicant's specification at page 6 lines 29-32). The Applicant's invention is directed both to mixed TDM and payload provisioning on the X-DSL communication channel as well as to synchronization of TDM frames on the sending and receiving modems. This latter objective is achieved using parameters loaded into each frame by the payload framer which allow the receiving modem to intermittently re-synchronize its TDM frames with the TDM frames of the sending modem, despite variations in the bit rate of the underlying X-DSL communication channel between the modems. These limitations found in each of amended Independent Claims 1,3 and 5 are not disclosed in and are therefore not anticipated by the Castellano reference. Amended dependent Claims 2,4 and 6 include the additional limitation of transport and synchronization of more than one TDM channel each with its own TDM slots, e.g. DSO's and with each TDM channel provisioned for either full T1 with 24 DSO's or fractional T1 with less than 24 DS)'s. This limitation is fully supported in the specification. (See for example FIG. 3A, 4 and Applicant's specification at

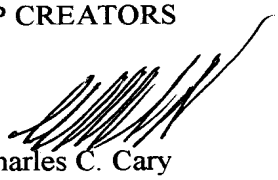
page 7 lines 1-13 and page 8, lines 3-7) This limitation is also not disclosed in the Castellano reference and is therefore not anticipated by same. Applicant therefore respectfully submits that Claims 1-6 has been placed in a condition for allowance.

CONCLUSION

In view of the above remarks, and the amendments to the Claims, Applicant believes that all remaining Claims 1-6 have been placed in a condition for allowance, and requests that they be allowed. Early notice to this effect is solicited.

The Commissioner is authorized to charge any additional fees which may be required, including petition fees and extension of time fees, to Deposit Account No. 50-1338 (Docket No. **VELCP005C**).

Respectfully submitted,
IP CREATORS



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